

09/52241.1 230000

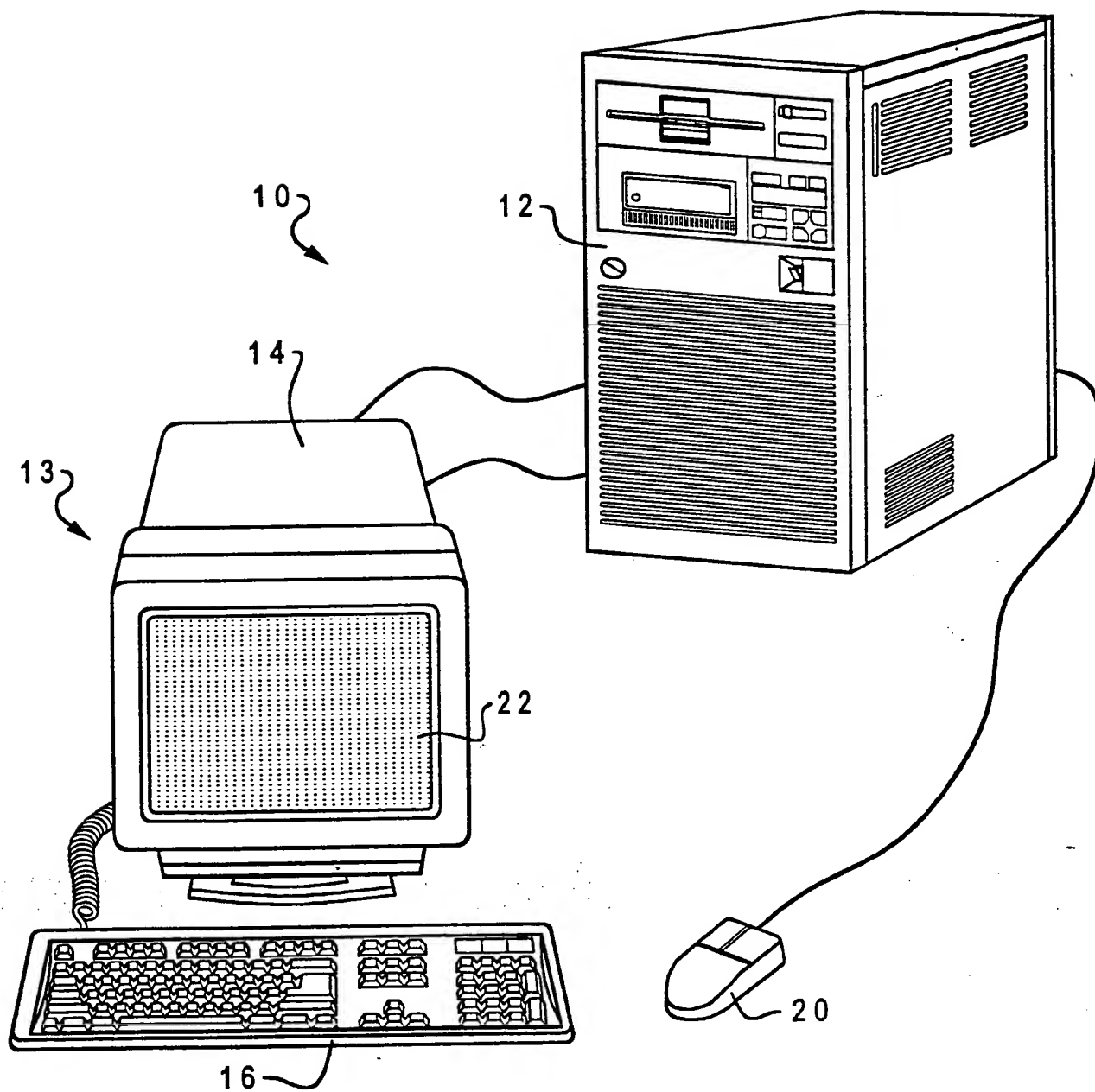


Fig. 1

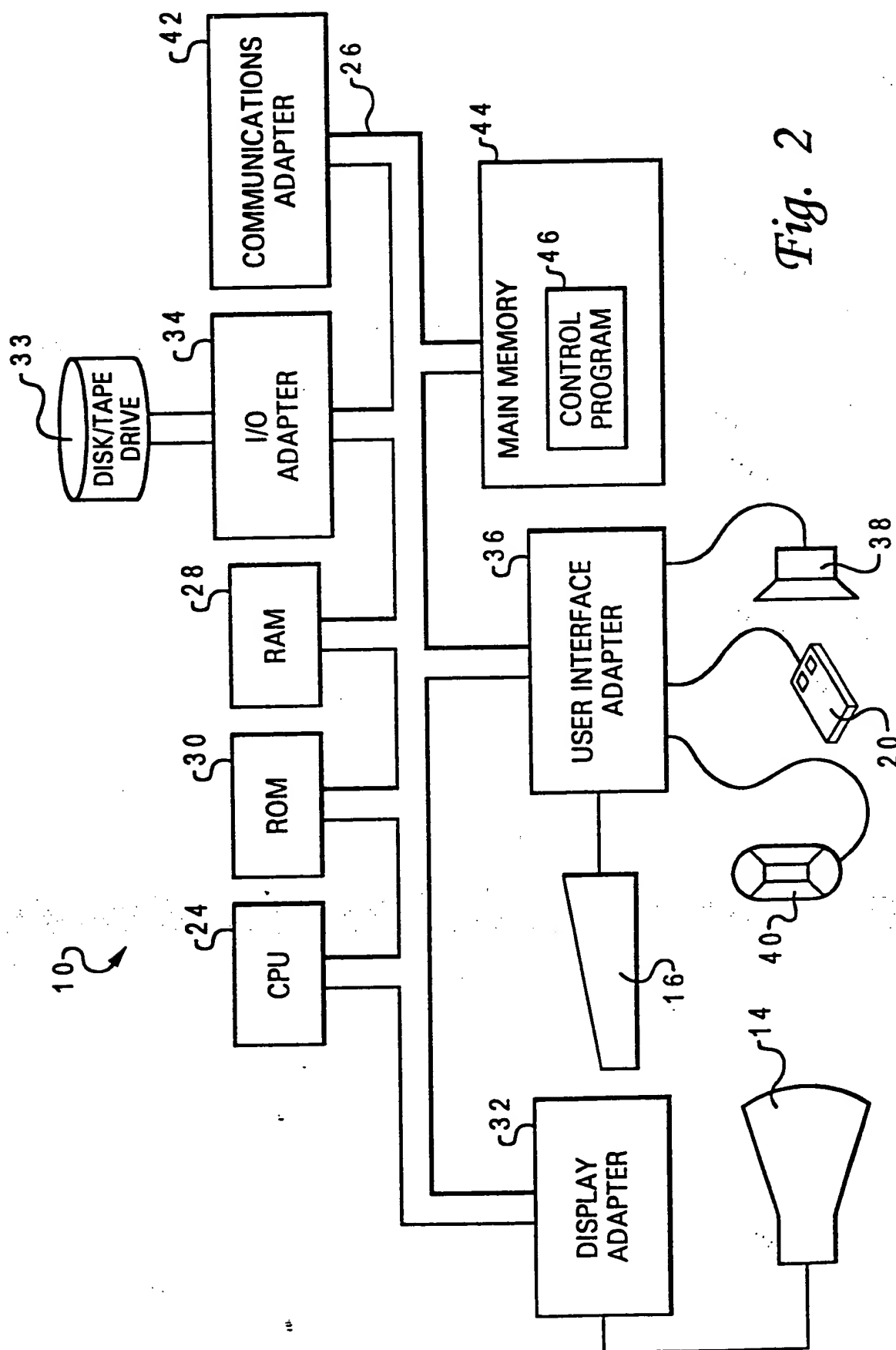


Fig. 2

300

301

303

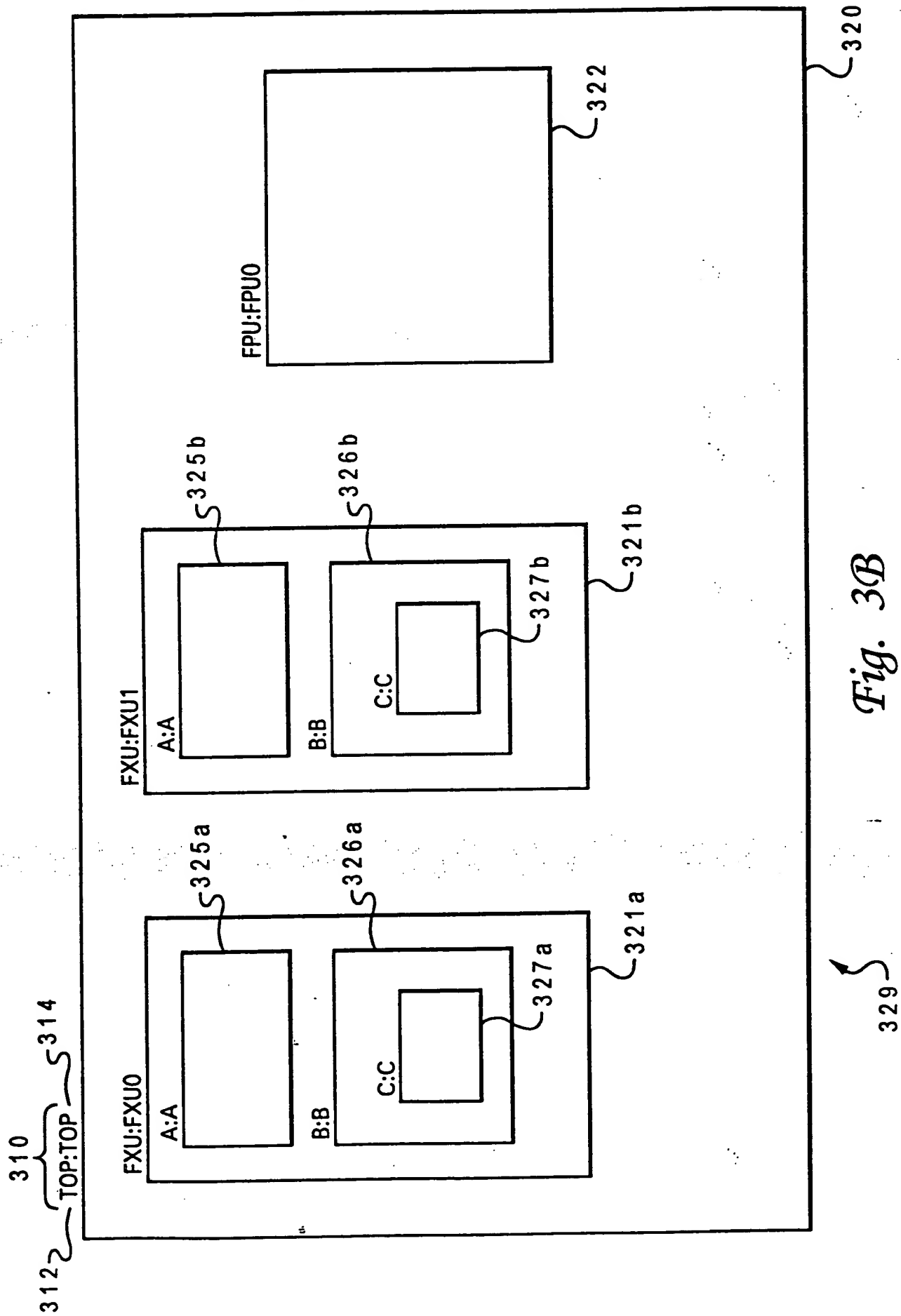
304

308

305

309

Fig. 3A



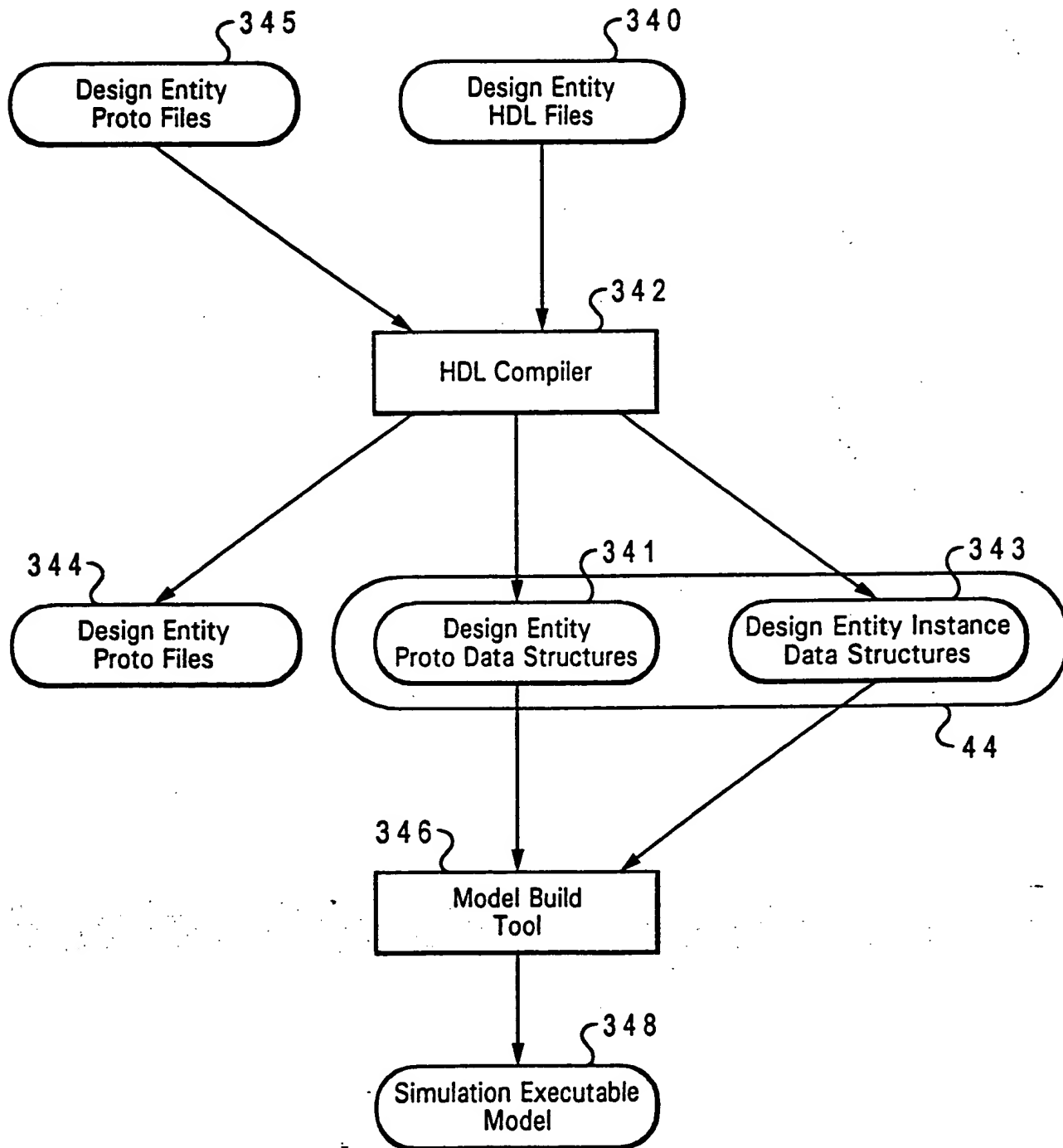


Fig. 3C

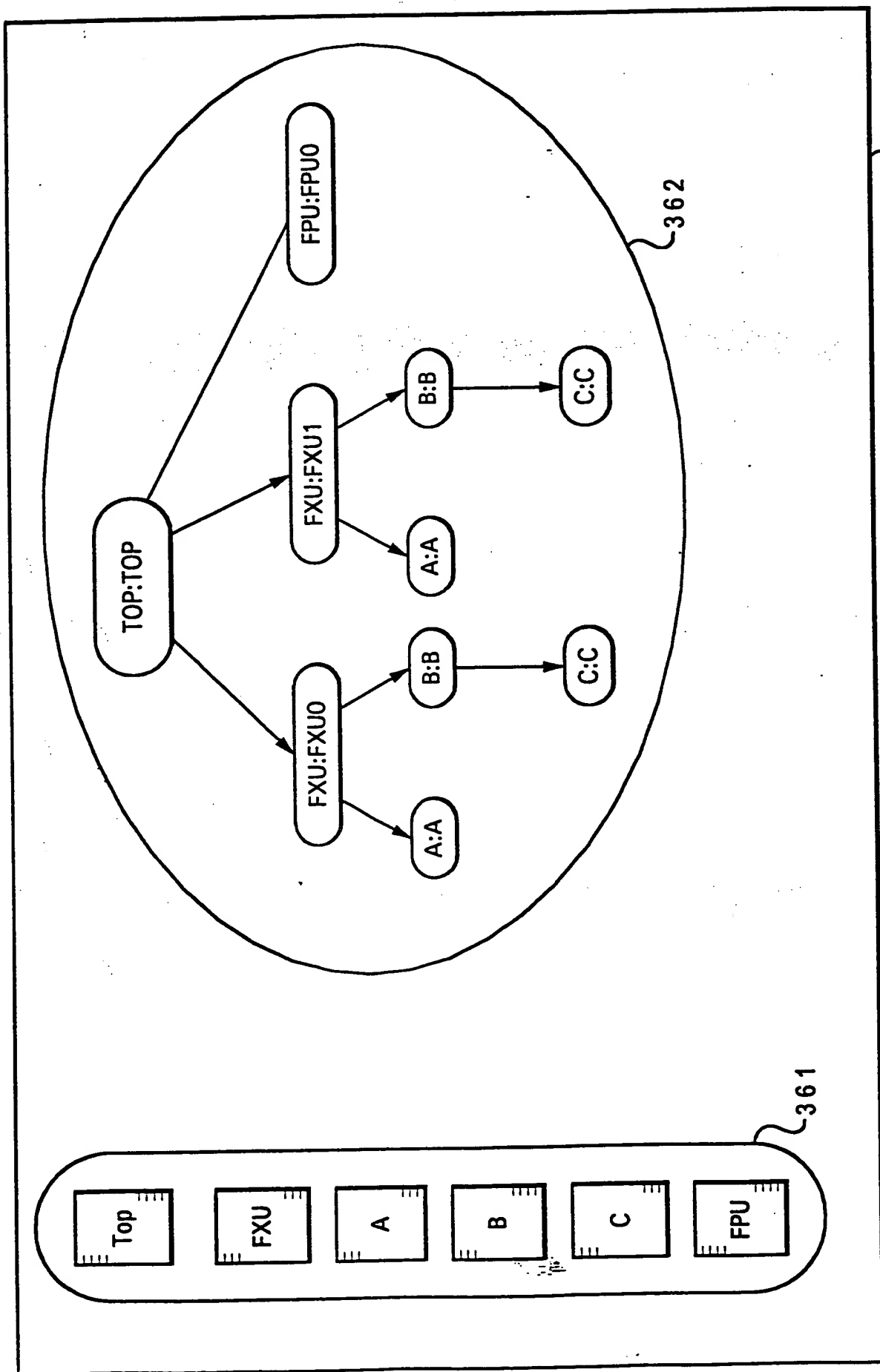


Fig. 3D

The diagram illustrates a system architecture. On the left, a series of horizontal arrows represent input data, passing through a lens-like component labeled 401. These arrows then pass through another lens-like component labeled 400. The output of this second component is a single arrow that enters a large, irregularly shaped block labeled 402. This block is situated within a larger rectangular frame labeled 409. From the right side of the block 402, three horizontal arrows emerge, labeled 403, 404, and 405. These arrows then pass through a series of three rectangular components labeled 406, 407, and 408, respectively. The final output is a single arrow labeled 409, which is the rightmost arrow in the sequence.

Fig. 4A

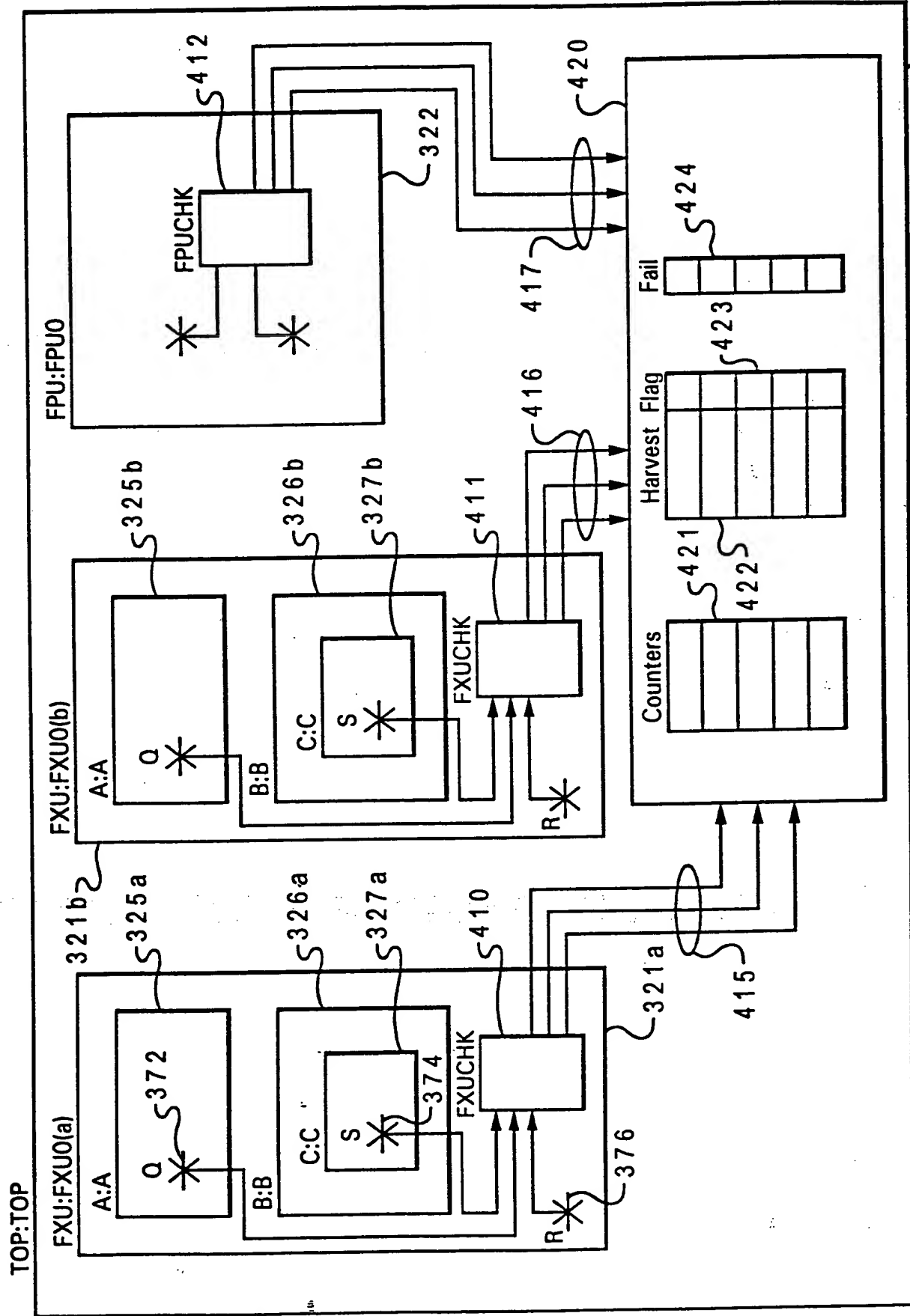


Fig. 4B

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Fig. 4C

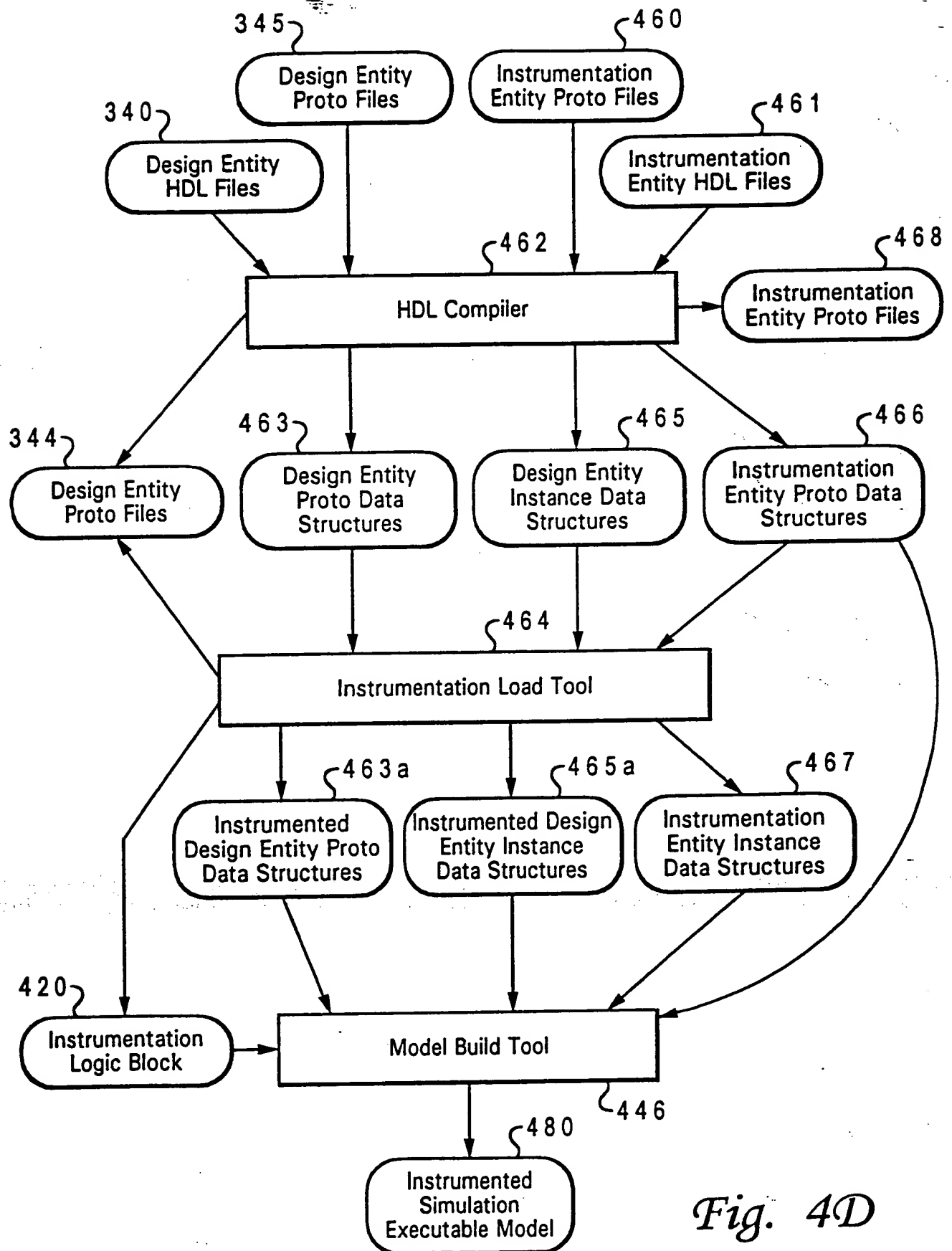


Fig. 4D

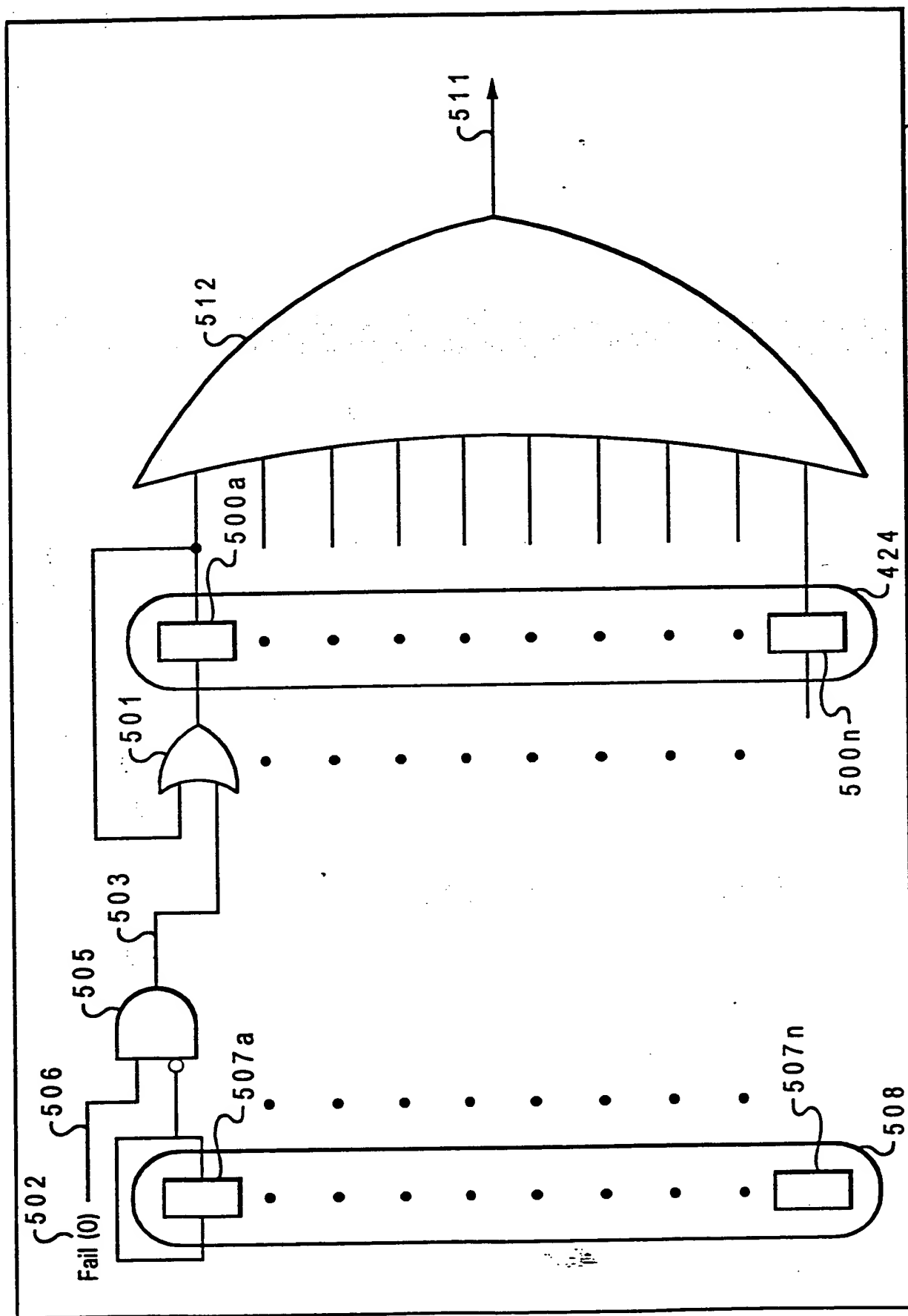


Fig. 5A

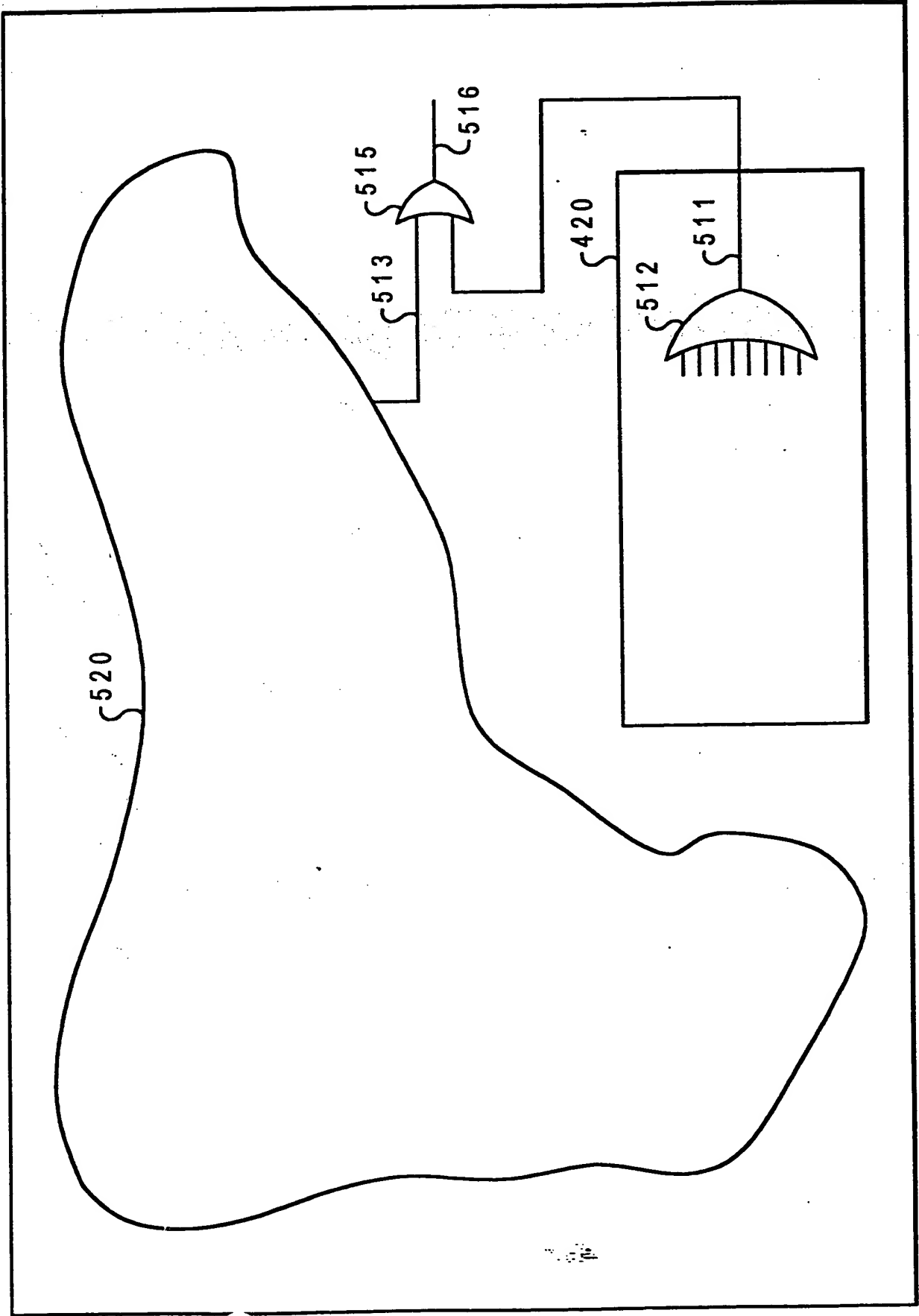


Fig. 5B

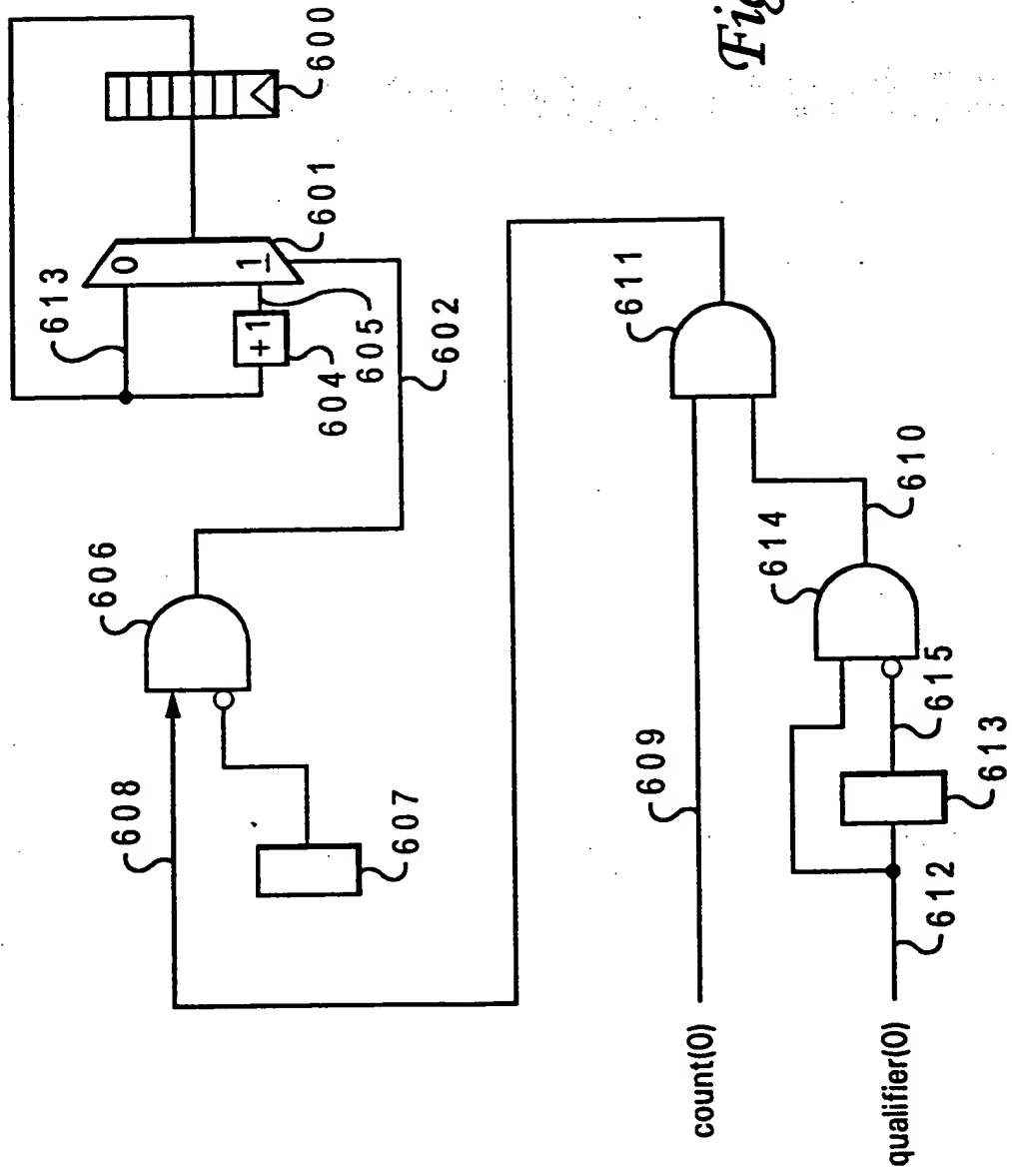
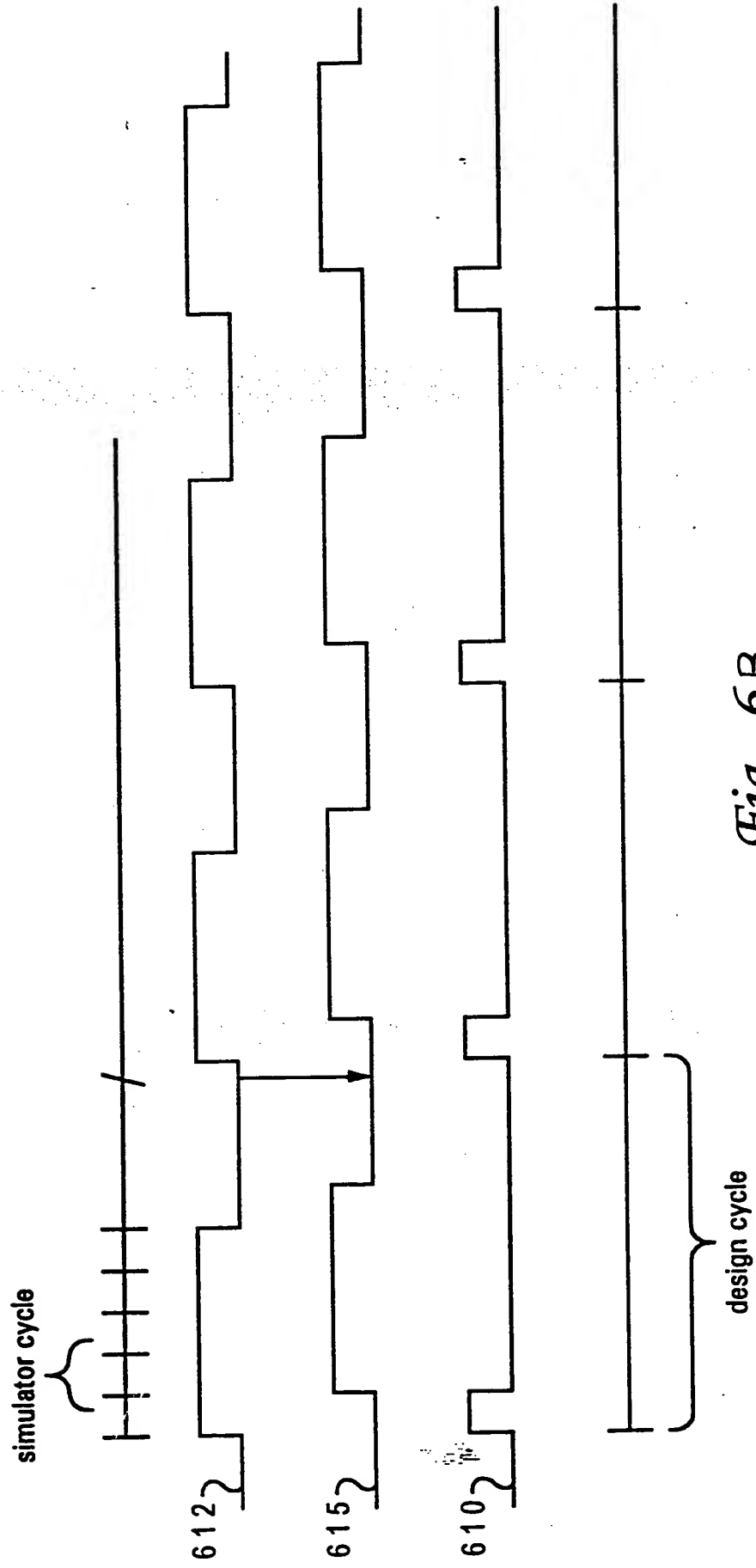


Fig. 6A



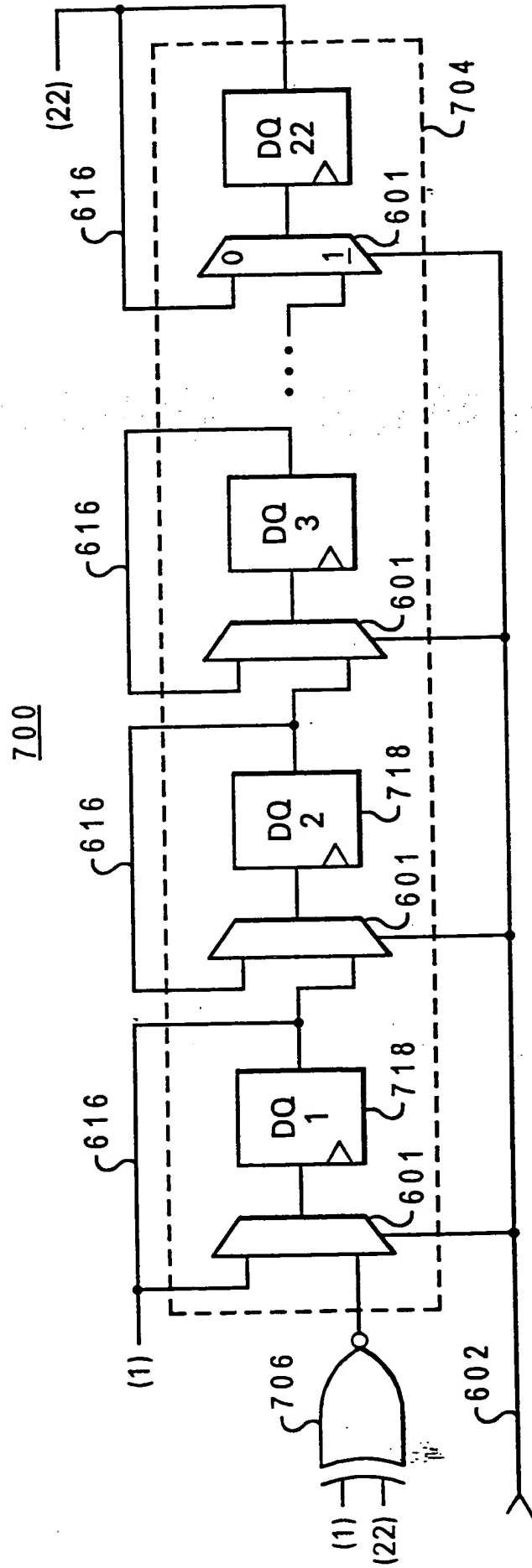


Fig. 7

entity Fsm: Fsm

850

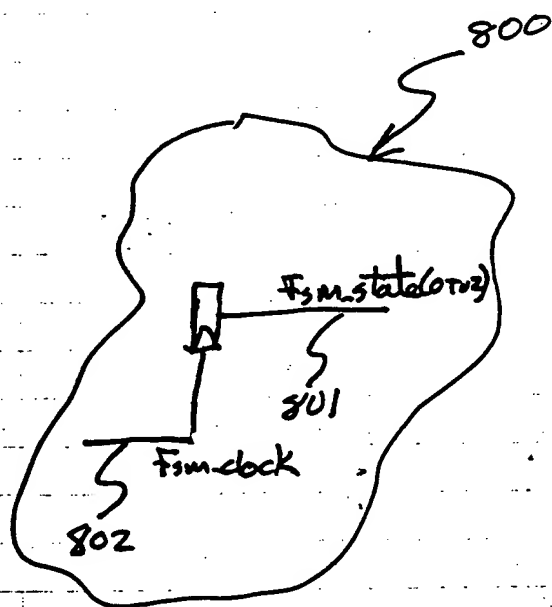


FIG. 8A
(Prior Art)

entity Fsm IS

PORT (

.... ports for entity Fsm

);

ARCHITECTURE Fsm OF Fsm IS

BEGIN

.... HDL code for Fsm and rest of the entity. ...

Fsm-state(0 to 2) <= ... signal 801

```
853 E  -- !! Embedded Fsm : exampleFsm;
854 E  -- !! clock       : (Fsm_clock);
855 E  -- !! state_vector : (Fsm_state(0 to 2));
856 E  -- !! states       : (s0, s1, s2, s3, s4);
857 E  -- !! state_encoding : ('000', '001', '010', '011', '100');
858 E  -- !! arcs         : (s0 => s0, s0 => s1, s0 => s2,
                           s1 => s2, s1 => s3, s2 => s2,
                           s2 => s3, s3 => s4, s4 => s0);
859 E  -- !! end Fsm;
```

852

END;

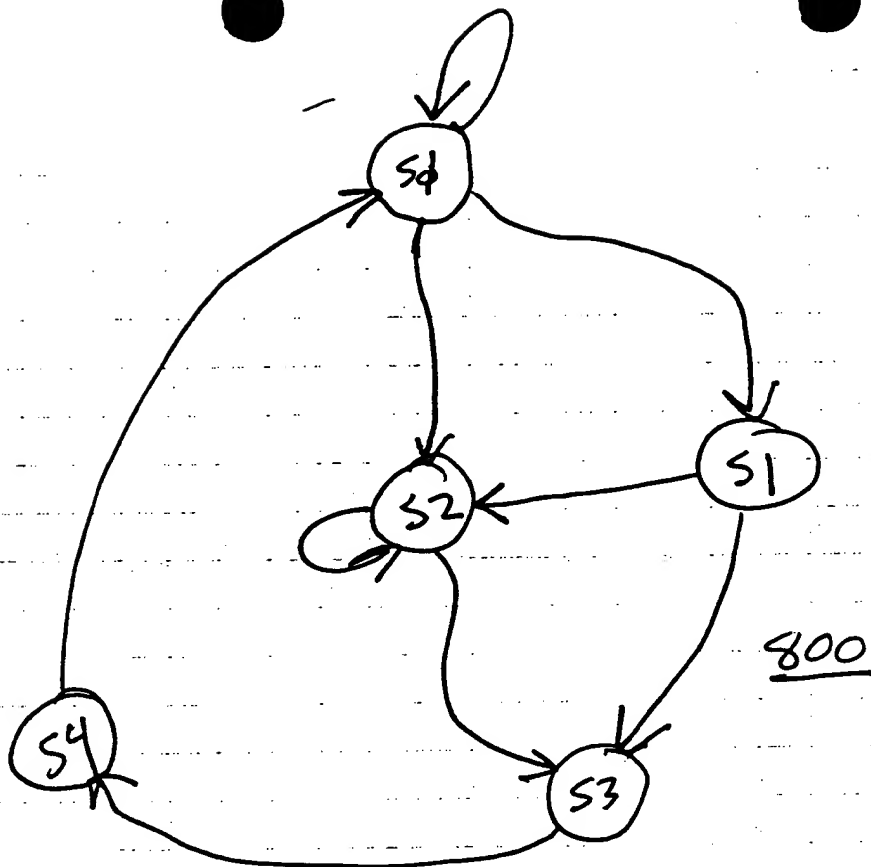


FIG. 8

(Prior Art)

entity FSM:FSM

850

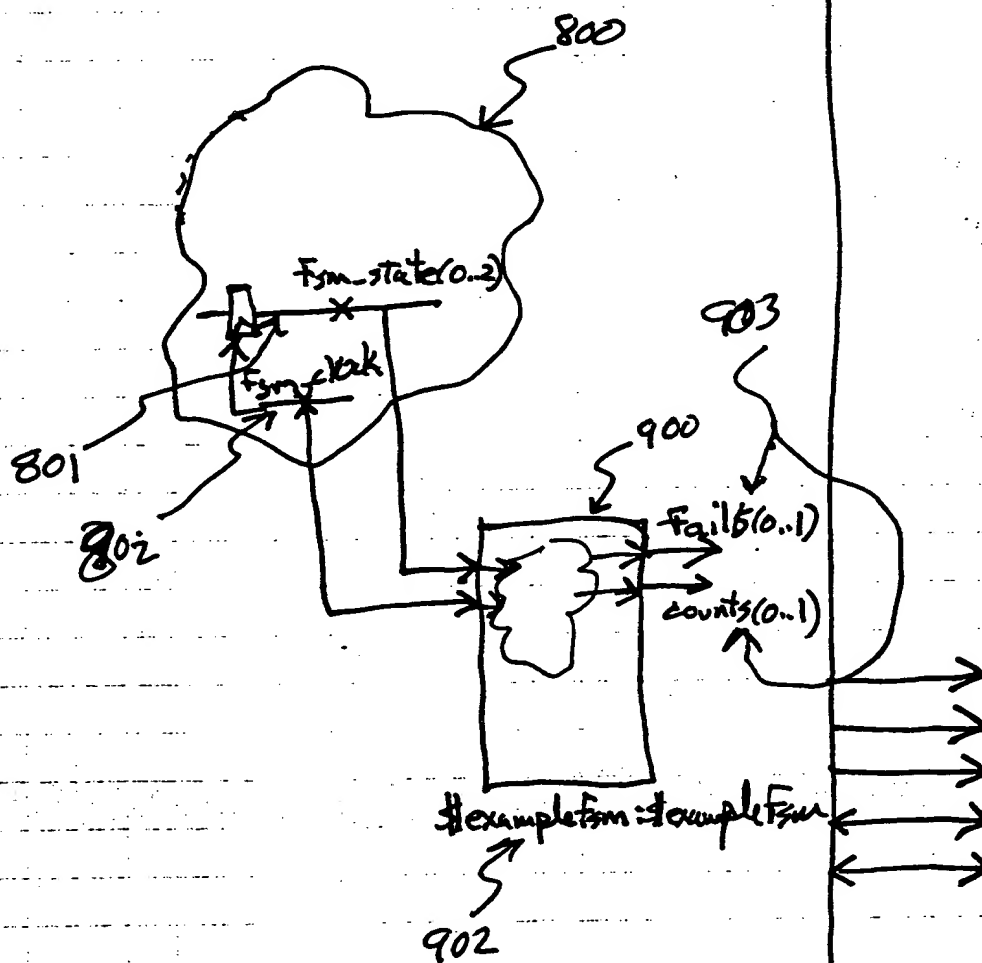


FIG. 9

TOP, TOP

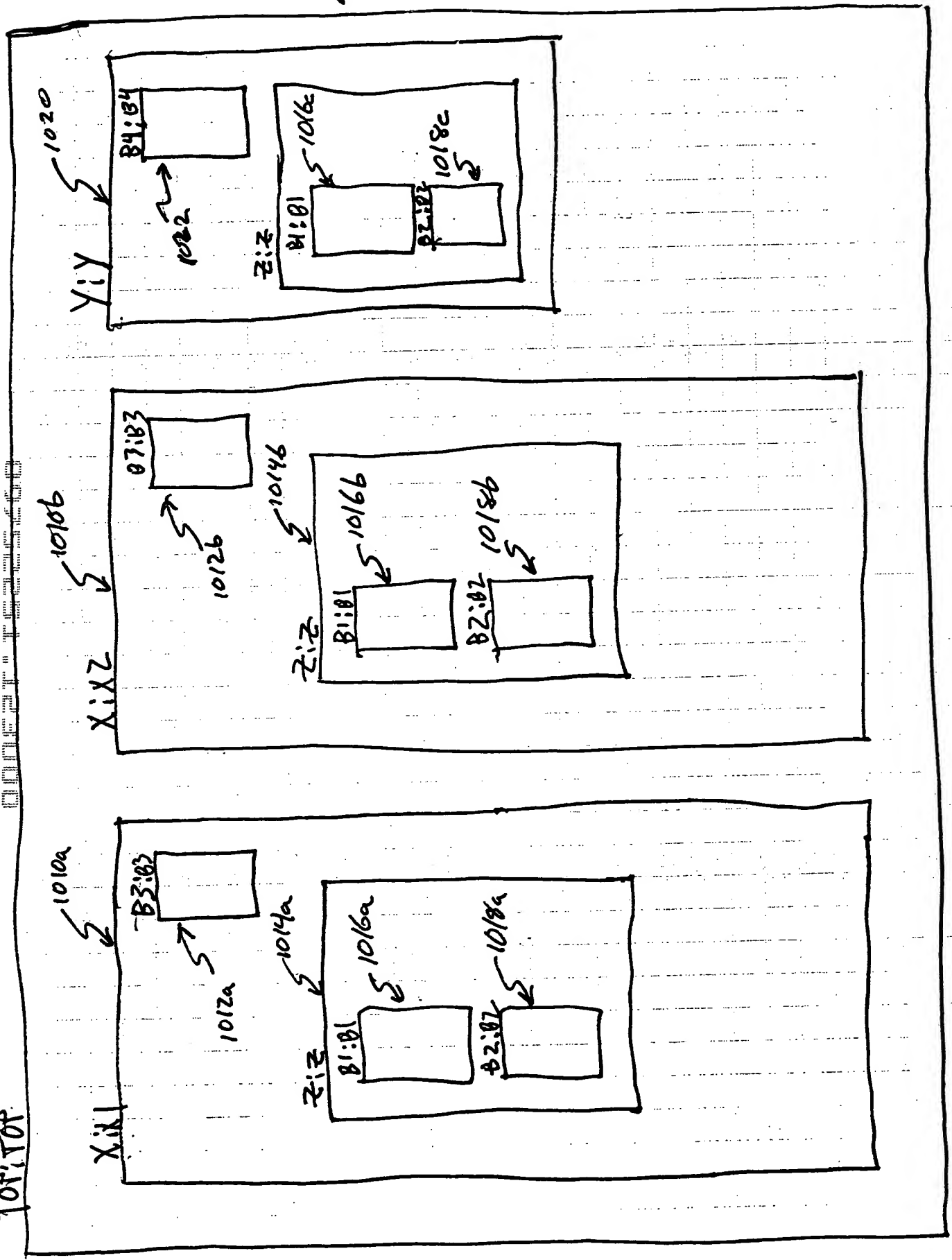


FIG. 10A

X:X

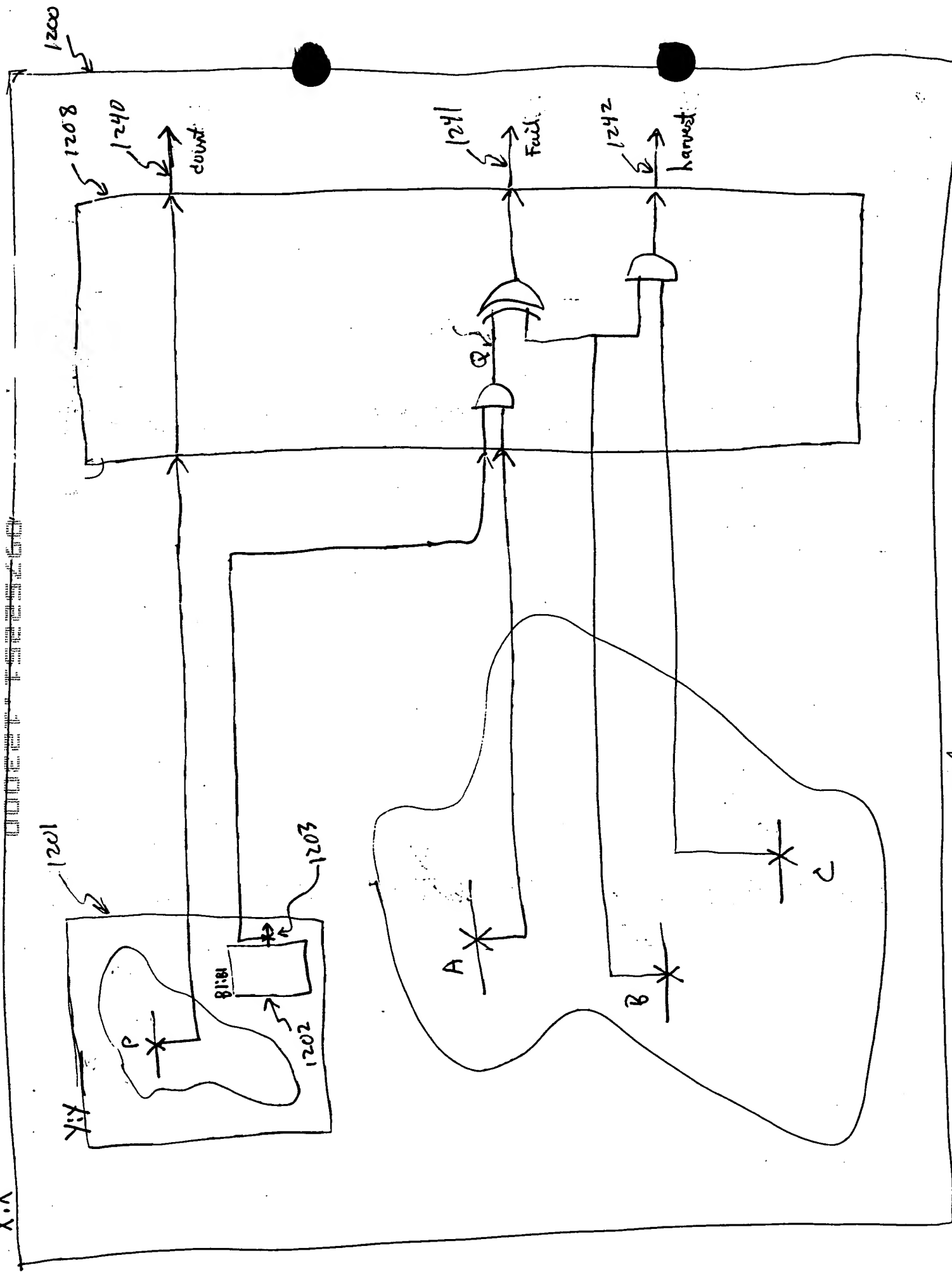


FIG. 12A 17A

Entity X IS

PORT (
;
);

ARCHITECTURE example OF X IS

BEGIN

...HDL CODE FOR X....

Y:Y
PORT MAP (
);

1221

A <= ...
B <= ...
C <= ...

1222

--!! [count, countname ϕ , clock] <= Y.P; } 1230
--!! Q <= Y.[B].count.count1 AND A; } 1232
--!! [fail, failname ϕ , "fail msg"] <= Q XOR B; } 1234
--!! [harvest, harvestname ϕ , "harvest msg"] <= B AND C; } 1236 } 1223

END

FIG. 12B